

Claims

- [c1] A method for manufacturing a semiconductor device, comprising steps of:
- forming a semiconductor layer on a substrate;
 - expanding a first region of the substrate to push up a first portion of the semiconductor layer;
 - compressing a second region of the substrate to pull down a second portion of the semiconductor layer;
 - forming an N type device over the first portion of the semiconductor layer; and
 - forming a P type device over the second portion of the semiconductor layer.
- [c2] The method of claim 1, further comprising a step of forming an oxide layer between the semiconductor layer and the substrate.
- [c3] The method of claim 1, wherein the step of expanding the first region comprises a step of ion-implanting an expansion element in the first region of the substrate.
- [c4] The method of claim 3, wherein the expansion element is ion-implanted at an implantation concentration of approximately 1×10^{14} atoms/cm² to 5×10^{16} atoms/cm²

and at an implantation energy of approximately 30 KeV to 300 KeV.

- [c5] The method of claim 3, wherein a concentration peak of the implanted expansion element is confined within the first region.
- [c6] The method of claim 3, wherein the expansion element is O_2 .
- [c7] The method of claim 3, wherein the step of compressing the second region comprises a step of ion-implanting a compression element in the second region of the substrate.
- [c8] The method of claim 7, wherein the compression element is ion-implanted at an implantation concentration of approximately 1×10^{14} atoms/cm² to 5×10^{16} atoms/cm² and at an implantation energy of approximately 30 KeV to 300 KeV.
- [c9] The method of claim 7, wherein a concentration peak of the implanted compression element is confined within the second region.
- [c10] The method of claim 7, wherein the compression element is He, Ar or noble gas.
- [c11] The method of claim 7, wherein the step of ion-

implanting the compression element comprise a step of masking to selectively expose a channel region of the P type device.

[c12] The method of claim 7, further comprising a step of annealing to expand the first region and to compress the second region.

[c13] The method of claim 12, wherein the step of annealing is performed at a temperature of approximately 500°C to 1200°C for approximately 1 second to 30 minutes.

[c14] A method of manufacturing a semiconductor device, comprising steps of:
forming a semiconductor layer on a substrate;
selectively ion-implanting an expansion element in a first region of the substrate;
selectively ion-implanting a compression element in a second region of the substrate;
annealing to expand the first region and to compress the second region, wherein the expanded first region pushes up a first portion of the semiconductor layer and the compressed second region pulls down a second portion of the semiconductor layer; and
forming an N type device on the first portion of the semiconductor layer; and forming a P type device on the second portion of the semiconductor layer.

- [c15] The method of claim 14, wherein the expansion element is O₂ and the compression element is He, Ar or noble gas.
- [c16] The method of claim 14, wherein the expansion element is ion-implanted at an implantation concentration of approximately 1×10^{14} atoms/cm² to 5×10^{16} atoms/cm² and at an implantation energy of approximately 30 KeV to 300 KeV.
- [c17] The method of claim 14, wherein the compression element is ion-implanted at an implantation concentration of approximately 1×10^{14} atoms/cm² to 5×10^{16} atoms/cm² and at an implantation energy of approximately 30 KeV to 300 KeV.
- [c18] The method of claim 14, wherein the step of annealing is performed at a temperature of approximately 500°C to 1200°C for approximately 1 second to 30 minutes.
- [c19] A semiconductor comprising:
a substrate comprising an expanded region and a compressed region;
a semiconductor layer formed on the substrate and comprising a first portion pushed up by the expanded region and a second portion pulled down by the compressed region;

an N type device formed on the first portion; and
a P type device formed on the second portion.

[c20] The semiconductor device of claim 19, further comprising an oxide layer formed between the semiconductor layer and the substrate.